Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-20 (canceled)

21. (New) A hardware-based multithreaded processor comprising:

a plurality of microengines, each of the microengines comprising:

a control store;

controller logic;

context event switching logic; and

an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the instructions causing the ALU to load a destination register with a 32-bit word formed by concatenating a first operand and a second operand to form a 64-bit result, shifting the 64-bit result by a specified amount, and storing a lower 32-bits of the 64-bit result.

22. (New) The processor of claim 21 wherein the first operand is a context-relative 32-bit register.

23. (New) The processor of claim 21 wherein the second operand is a context-relative 32-bit register.

24. (New) The processor of claim 21 wherein the shifting is a right shifting.

25. (New) The processor of claim 21 wherein the destination register is an absolute register name.

26. (New) The processor of claim 21 wherein the destination register is a context relative register name.

27. (New) The processor of claim 21 wherein the destination register is a context-relative 32-bit register.

28. (New) The processor of claim 21 wherein the specified amount is a value contained in the first operand.

29. (New) The processor of claim 21 wherein the specified amount is a value contained in a lower five bits of the first operand.

30. (New) The processor of claim 21 wherein the specified amount is a value representing a right shift of values from 1 to 31.